CLAIMS

What is claimed is:

1. A method for improving charge mobility in a MOSFET device comprising the steps of:

providing a first gate with a first semiconductor conductive type and a second gate with a second semiconductor conductive type overlying a substrate;

forming a first strained layer with a first type of stress overlying said first gate; and,

forming a second strained layer with a second type of stress overlying said second gate.

2. The method of claim 1, further comprising the step of transferring the first stress type from the first strained layer to the first gate and the second stress type from the second strained layer to the second gate.

3. The method of claim 1, further comprising the step of removing the first and second strained layers.

4. The method of claim 1, wherein an oxide layer is formed over the first and second gates prior to the steps of forming a first and second strained layer.

5. The method of claim 1, wherein an ion implantation process to form dopant regions including forming an amorphous portion in the first and second gates prior to the steps of forming a first and second strained layer.

6. The method of claim 5, further comprising the step of carrying out an annealing process to recrystallize the amorphous portion following the steps of forming a first and second strained layer.

7. The method of claim 1, wherein the first and second stress types are selected from the group consisting of tensile stress and compressive stress formed over a respective N conductive type gate and P conductive type gate.

8. The method of claim 1, wherein the steps of forming a first and second strained layer comprise the steps of:

forming the first strained layer;

removing a first portion of the first strained layer over one of the first and second gates to leave an uncovered portion; and,

forming the second strained layer over the uncovered portion.

9. The method of claim 1, wherein the first and second strained layers are deposited by a CVD process selected from the group consisting of LPCVD, ALCVD, and PECVD.

10. The method of claim 1, wherein the first and second strained layers comprise a nitride.

11. The method of claim 1, wherein the wherein the first and second strained layers are selected from the group consisting of silicon nitride and silicon oxynitride.

12. The method of claim 1, wherein the wherein the first and second strained layers comprise a stress level up to about 2 GPa.

13. The method of claim 1, wherein the first and second strained layers are formed at a thickness from about 50 Angstroms to about 1000 Angstroms.

14. The method of claim 1, wherein the steps of forming the first and second strained layers is carried out at a temperature less than about 600 °C.

15. A method for improving charge mobility in a MOSFET device comprising the steps of:

providing a first gate with a first semiconductor conductive type and a second gate with a second semiconductor conductive type overlying a substrate;

forming a first strained layer with a first type of stress overlying said first gate;

forming a second strained layer with a second type of stress overlying said second gate;

transferring the first stress type from the first strained layer to the first gate and the second stress type from the second strained layer to the second gate; and,

removing the first and second strained layers.

16. A method for improving charge mobility in a MOSFET device comprising the steps of:

providing a substrate comprising at least one polysilicon gate electrode;

performing an ion implantation process to form dopant regions including forming an amorphous portion in the at least one polysilicon gate electrode;

forming a first dielectric layer comprising a selected stress level selected from the group consisting of tensile stress and compressive stress over the at least one polysilicon gate electrode; and,

carrying out an annealing process to recrystallize the amorphous portions of the respective polysilicon gate electrodes to form a stress level in the substrate.

17. A method for improving charge mobility in a MOSFET device comprising the steps of:

providing a substrate comprising at least one polysilicon gate electrode;

performing an ion implantation process to form dopant regions including forming an amorphous portion in the polysilicon gate electrode; and,

forming at least one dielectric layer comprising a selected stress level selected from the group consisting of tensile stress and compressive stress over the at least one polysilicon gate electrode.

18. The method of claim 17, further comprising carrying out an annealing process to recrystallize the amorphous portion and activate the dopant regions while forming a stress level in the substrate.

19. The method of claim 17, wherein the step of forming a dielectric layer further comprises forming an underlying oxide layer.

20. The method of claim 17, wherein the step of forming at least one dielectric layer comprises forming a dielectric layer in tensile stress over an N-type polysilicon gate electrode and a dielectric layer in compressive stress over a P-type polysilicon gate electrode.

21. The method of claim 20, comprising the steps of:

forming a first dielectric layer comprising a first stress type selected from the group consisting of tensile and compressive stress;

removing a first portion of the first dielectric layer over one of the N-type and P-type polysilicon gate electrodes; and,

forming a second dielectric layer comprising a second stress type opposite from the first stress type over the first portion.

22. The method of claim 17, wherein the at least one dielectric layer is formed by a CVD process selected from the group consisting of LPCVD, ALCVD, and PECVD.

23. The method of claim 17, wherein the at least one dielectric layer comprises a nitride.

24. The method of claim 17, wherein the at least one dielectric layer is selected from the group consisting of silicon nitride and silicon oxynitride.

25. The method of claim 17, wherein the stress level is formed at up to about 2 GPa.

26. The method of claim 17, wherein the at least one dielectric layer is formed at a thickness from about 50 Angstroms to about 1000 Angstroms.

27. The method of claim 17, further comprising the step of removing at least a portion of the least one dielectric layer.

28. The method of claim 27, further comprising the step of forming a silicide region in the uppermost portion of the polysilicon gate electrode.

29. The method of claim 17, wherein the step of forming the at least one dielectric layer is carried out at a temperature less than a recrystallization temperature of the amorphous portion.

30. The method of claim 17, wherein the step of forming at least one dielectric layer is carried out at a temperature less than about 600 °C.

31. A MOSFET device pair with improved charge mobility comprising:

a first gate with a first semiconductor conductive type and a second gate with a second semiconductor conductive type overlying a substrate;

a first strained layer with a first type of stress overlying said first gate; and,

a second strained layer with a second type of stress overlying said second gate.

32. The MOSFET device pair of claim 31, wherein the first and second gates comprise a respective N semiconductor conductive type and P semiconductor conductive type with a respective overlying tensile stress type first strained layer and compressive stress type second strained layer.

33. The MOSFET device pair of claim 31, further comprising an oxide layer interposed between the first and second strained layers and the respective first and second gates.

34. The MOSFET device pair of claim 31, wherein the first and second gates further comprise recrystallized polysilicon.

35. The MOSFET device pair of claim 31, wherein the first and second strained layers comprise a nitride.

36. The MOSFET device pair of claim 31, wherein the first and second strained layers are selected from the group consisting of silicon nitride and silicon oxynitride.

37. The MOSFET device pair of claim 31, further comprising a strained channel region in the semiconductor substrate underlying the respective first and second gates comprising a strain transferred from at least one of the respective first and second gates and the first and second strained layers.

38. The MOSFET device pair of claim 31, wherein the wherein the first and second strained layers comprise a stress level up to about 2 GPa.

39. The MOSFET device pair of claim 31, wherein the first and second strained layers are formed at a thickness from about 50 Angstroms to about 1000 Angstroms.

40. Strained channel MOSFET devices with improved charge mobility comprising:

a semiconductor substrate comprising N type and P type conductivity polysilicon gate electrodes;

a first strained dielectric layer having primarily a tensile stress overlying the N type conductivity gate electrodes and a second strained dielectric layer having primarily a compressive stress overlying the P type conductivity gate electrodes; and,

strained channel regions in the semiconductor substrate underlying the respective polysilicon gate electrodes comprising a strain transferred from at least one of the respective polysilicon gate electrodes and the respective first and second strained layers.

41. The strained channel MOSFET devices of claim 40, further comprising an oxide layer interposed between the respective polysilicon gate electrodes and the respective first and second strained dielectric layers.

42. The strained channel MOSFET devices of claim 40, wherein the N type and P type conductivity polysilicon gate electrodes comprise recrystallized polysilicon.

43. The strained channel MOSFET devices of claim 40, wherein the first and second strained dielectric layers are selected from the group consisting of silicon nitride and silicon oxynitride.